FPGAs in 2032: Challenges and Opportunities in the next 20 years

Convergence of Programmable Solutions

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Tempting Topic Not Discussed Here

Predictions from 1992 about 2012

- Accurate ones
- Hilarious ones
- Probably more accurate than now predicting 2032

1990s

<table>
<thead>
<tr>
<th>Glue Logic</th>
<th>Heterogeneous Capabilities</th>
<th>High Integration/Bandwidth</th>
<th>Hardened Subsystems</th>
<th>Cortex-A9 MPCore</th>
</tr>
</thead>
<tbody>
<tr>
<td>Flex 6000 3µ process</td>
<td>Stratix I 130nm process</td>
<td>Stratix IV 40nm process</td>
<td>Stratix V 28nm process</td>
<td>SoC FPGA 28nm process</td>
</tr>
</tbody>
</table>

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A controllable transistor engineered from a single phosphorus atom has been developed by researchers at the University of New South Wales, Purdue University and the University of Melbourne. The atom, shown here in the center of an image from a computer model, sits in a channel in a silicon crystal. (Credit: Purdue University)
Tempting Topic Not Discussed Here

DNA computing

- Scientists at IBM are experimenting with using DNA molecules as a way to create tiny circuits that could form the basis of smaller, more powerful computer chips.
Tempting Topics Not Discussed Here

Conventional Devices

FET

Band gap engineered
Graphene nanoribbons

Graphene quantum dot

(Manchester group)

Nonconventional Devices

Graphene Veselago lense

Cheianov et al. Science (07)

Graphene Spintronics

Son et al. Nature (07)

Graphene pseudospintronics

Trauzettel et al. Nature Phys. (07)

P. Kim – Columbia U.
Tempting Topics Not Discussed Here

- Wonderful applications of technology in 2032
  - 6 billion connected people
  - 100 billion connected devices
    - Internet of Things
  - Wearable electronics
  - Genome informatics and personalized medicine
  - Intelligent robots and machines
    - Singularity
  - Many others…
Topics Discussed Today

- Convergence of programmable platforms
- A need for programming models, languages and compilers for converged programmable platforms
- Summary
ITRS Roadmap Ends In 2026
Intel 22nm FinFET Announced May 2011

Claimed benefits relative to 32nm:
- 18% faster at 1.0V, 37% faster at 0.7V
- 50% lower power at same performance
- 2-3% higher cost than planar process
“More Moore” Projections

<table>
<thead>
<tr>
<th>Year</th>
<th>2012</th>
<th>2014</th>
<th>2017</th>
<th>2020</th>
<th>2023</th>
<th>2026</th>
<th>2029</th>
<th>2032</th>
</tr>
</thead>
<tbody>
<tr>
<td>Node</td>
<td>20nm</td>
<td>14nm</td>
<td>10nm</td>
<td>7nm</td>
<td>5nm</td>
<td>3.5nm</td>
<td>2.5nm</td>
<td>1.8nm</td>
</tr>
<tr>
<td># FETs per die (B)</td>
<td>8</td>
<td>14</td>
<td>28</td>
<td>56</td>
<td>113</td>
<td>222</td>
<td>453</td>
<td>887</td>
</tr>
<tr>
<td>M1 1/2 pitch (nm)</td>
<td>32</td>
<td>24</td>
<td>16.9</td>
<td>11.9</td>
<td>8.4</td>
<td>6</td>
<td>4.2</td>
<td>3</td>
</tr>
<tr>
<td>Lgate (nm)</td>
<td>22</td>
<td>18</td>
<td>14</td>
<td>10.6</td>
<td>8.1</td>
<td>5.9</td>
<td>4.2</td>
<td>3</td>
</tr>
</tbody>
</table>

* Normalized to 20nm

- Sources: ITRS 2010, ITRS 2011, Altera projections beyond 2026
2032 Process Technology Extrapolation

- “More Moore” scaling produces:
  - ~1 Trillion transistors per die, >100X of 20nm technology
  - 250X increase in throughput compared to 20nm
  - Minimum features of ~13X silicon atomic spacing
  - Faster transistors, but much slower interconnect

- Many significant challenges exist
  - New materials and device structures are necessary
    - Long term options: Tunnel FET, nano wires, graphene, non-CMOS devices

- Slower scaling combined with 3D is an attractive alternative

- More Than Moore can achieve same transistor count as More Moore
IMEC 3D System Integration Program

Logic IDM
- Panasonic
- Intel
- Fujitsu
- Sony

Memory IDM
- Micron
- Samsung

Foundries
- GLOBALFOUNDRIES

OSAT
- TSMC

Material Suppliers
- BASF
- Hitachi Chemical
- Thin Materials
- Henkel

Fabless
- Qualcomm
- Xilinx
- Altera
- NVIDIA

EDA
- Synopsys
- Cadence

Equipment Suppliers
- Applied Materials
- Lam Research
- TOKYO ELECTRON
- Suss Microtec
- Cascade Microtech
- Ultratech
- NandaTech

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3D Integration Technology Opportunities

- ADC / DAC
- Optical
- ASSP
- Memory
- ASIC
- M-core CPU
- XCVR + FPGA

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13
Programmable Platforms in 2012

Moore’s law has enabled a range high density programmable platforms

- CPUs
- DSPs
- Multi-Cores
- Many-Core Arrays
- FPGAs

Single Cores
Multi-Cores
Coarse-Grained CPUS and DSPs
Coarse-Grained Massively Parallel Processor Arrays
Fine-Grained Massively Parallel Heterogeneous Arrays
Augmenting Fine-Grained Fabric with Coarse-Grained Programmable Functions in FPGAs
Emerging SoC FPGAs

- **Processor**
  - Dual ARM Cortex-A9
- **SDRAM Controller, Peripherals**
- **Other Hard IP**
  - Serial protocols, memory interfaces
- **FPGA programmable fabric**
  - Multiple density options
- **Programming model: C/C++ for ARM**
  - Common operating systems
  - APIs for hardware accelerators developed in HDL (Verilog, VHDL, System Verilog), or C/C++ by using high-level-synthesis
  - OpenCL

* * Integrated DMA logic
From 2022 to 2032 all SoCs will be programmable, a combination of today’s architectures.
Emerging Parallel Programming Models

- Parallel programming is still evolving for many-cores
- OpenCL emerging for many-cores, FPGAs and SOC FPGAs

- CUDA, OpenCL for GPUs,
- Versions of C, C++ and bare-metal programming for many-cores

- OpenCL parallel programming for FPGAs and SOC FPGAs
- C/C++ for ARM with OpenCL for implementing and managing hardware accelerators
OpenCL Compiler for FPGAs

__kernel void
sum(__global const float *a,
__global const float *b,
__global float *answer)
{
    int xid = get_global_id(0);
    answer[xid] = a[xid] + b[xid];
}

int xid = get_global_id(0);
answer[xid] = a[xid] + b[xid];
Monte Carlo simulation of all possible paths for the underlying equity value
Summary

Key directions to 2022 and 2032

- Convergence of programmable platforms
  - Heterogeneous architectures
- Programming models and compilers for the converged programmable platforms
Thank You